ABSTRACT OF DISCLOSURE

A method of fabricating an exposure mask for semiconductor manufacture to improve the accuracy of critical dimensions of the mask pattern. The method includes the steps of forming a chrome layer, a first photo resist, a conductive layer and a second photo resist on a transparent quartz substrate, in sequence; forming a second photo resist pattern by exposing and developing the second photo resist; forming a conductive layer pattern by etching the conductive layer using the second photo resist pattern as an etch barrier; removing the second photo resist pattern; forming an oxide layer as a layer for shielding light at the surface of the conductive layer pattern by oxidizing the conductive layer pattern; exposing the first photo resist using the conductive layer pattern having the oxide layer at the surface thereof; forming a first photo resist pattern exposing the chrome layer by developing the exposed first photo resist; forming a mask pattern including the chrome layer by selectively etching the exposed chrome layer parts; and removing the conductive layer pattern including the oxide layer and the first photo resist pattern.